REMARKS

Claim 6 has been amended to correct a typographical error. Claims 1-4, 6, and 8-19 are pending in the captioned case. Further examination and reconsideration of the presently claimed application are respectfully requested.

Allowable Subject Matter

Claim 17 was deemed allowable if rewritten into independent form including all of the limitations of the base claim and any intervening claims. Applicants appreciate the Examiner's recognition of allowable subject matter. However, for reasons set forth below, it is believed that the independent claims and claims dependent therefrom are allowable in their present form over the art of record.

Objection to the Claims

An objection was lodged against claim 6 for a typographical error. In response thereto, claim 6 has been amended to correct its dependency. Accordingly, Applicants believe this objection has been obviated.

Section 103 Rejection

Claims 1-4, 6, 8-16, and 18-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,906,871 to Iida (hereinafter "Iida"). To establish a case of *prima facie* obviousness of a claimed invention, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. Second, there must be a reasonable expectation of success. As stated in MPEP 2143.01, the fact that references can be hypothetically combined or modified is not sufficient to establish a *prima facie* case of obviousness. *See In re Mills*, 916 F.2d. 680 (Fed. Cir. 1990). Finally, the prior art references must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d. 981 (CCPA 1974); MPEP 2143.03. Specifically, "all words in a claim must be considered when judging the patentability of that claim against the prior art." *In re Wilson* 424 F.2d., 1382 (CCPA 1970). Using these

standards, Applicants contend that the cited art fails to teach or suggest all features of the currently pending claims, some distinctive features of which are set forth in more detail below.

Iida does not suggest or provide motivation for a transmission gate having a gate terminal of a p-channel transistor coupled to a power supply voltage and a gate terminal of a n-channel transistor coupled to a ground supply voltage during power down of the circuit. Present claim 1 indicates various voltages placed on the gate terminals of transistors which form the transmission gate during power down of the circuit. Specifically, the p-channel transistor gate terminal is coupled to a power supply voltage and the n-channel transistor gate is coupled to a ground supply voltage during a specific time known as the power down time.

Contrary to claim 1, Iida specifically discloses the opposite to that which is claimed. For example, Iida denotes the p-channel transistor Q8 is coupled to a ground supply voltage, and the n-channel transistor Q7 is coupled to a power supply voltage (Iida -- Fig. 7). As further described in Iida, in order to form a bias resistor R5, both transistors Q7 and Q8 must be in a conductive state (Iida -- col. 4, lines 62-66). In order to place transistors Q7 and Q8 in a conductive state, the p-channel transistor must have its gate grounded and the n-channel transistor must have its gate connected to a power supply (Iida -- col. 4, lines 34-44). The teachings of Iida that the n-channel transistor gate be coupled to a power supply and the p-channel transistor gate be coupled to a ground supply is exactly the opposite of that which is presently claimed. The purpose of Iida is to render the transistors of the transmission gate conductive. No motivation is provided anywhere in Iida for reversing the conductive state of those transistors and, specifically, to reverse the conductive state of the transistors during a power down timeframe.

Iida must suggest the desirability of the present claims or must at least show to a skilled artisan a motivation to modify Iida to arrive at present claim 1. MPEP 2143.01. Absent any suggestion or motivation in Iida and, in fact, when it teaches away from the present claim 1, Iida cannot be used to support a *prima facie* case of obviousness. Essentially, teaching away from the art is a *per se* demonstration of lack of *prima facie* obviousness. *In re Dow Chemical Co.*, 837 F.2d. 469 (Fed. Cir. 1988). When examining Iida, a skilled artisan would maintain the transmission gate always in the conductive state and would not be motivated to modify that state at any time, and certainly would not be motivated to render the transmission gate in a non-conductive state during a power down operation. Accordingly, Applicants assert that independent claim 1 and claims dependent therefrom are not obvious over Iida.

Iida does not suggest or provide motivation for a biasing circuit coupled to an input of each of a pair of inverters, or a pair of capacitors coupled between the pair of inverters and the respective pair of outputs of a differential amplifier. Present claim 11 describes a receiver that has a pair of inverters, a biasing circuit coupled to the inputs of each of the pair of inverters, and a pair of capacitors coupled between the pair of inverters and respective pair of outputs of the differential amplifier. Accordingly, claim 11 requires a double-ended output of the differential amplifier be biased using two inverters, two biasing circuits, and two capacitors arranged in the claimed fashion.

Contrary to the double-ended features of claim 11, Iida only teaches use of a single-ended output from resistor R3. Thus, only a single capacitor, a single inverter, and a single biasing circuit is shown, described, or suggested in Iida (Iida – Fig. 3). In fact, Iida specifically teaches away from replicating the circuit to provide a double-ended output, since the purpose of Iida is to "provide a level shift circuit which requires a reduced number of circuit elements" compared to that of the prior art circuit of Fig. 1 which has a double-ended output, but absent a biasing circuit and capacitor at each output (Iida -- col. 1, lines 54-56, emphasis added; Figs. 1 and 3 in comparison). Moreover, Iida explicitly states that "it is noted here that the level shift circuit is made up of only capacitor 19, CMOS inverter 20, and the bias circuit or resistor R5" (Iida – col. 4, lines 18-21, emphasis added). Iida continues by noting the level shifter of Fig. 3, when compared to that shown in Fig. 1, requires less number of circuit elements -- the primary goal of Iida (Iida -- col. 4, lines 22-25).

Since Iida appears to specifically require only a single-ended output with fewer circuit elements, nowhere in Iida is there any suggestion for modifying its purpose to having a double-ended output with more circuit elements. Accordingly, Applicants assert that independent claim 11 and claims dependent therefrom are not obvious over Iida.

Iida does not suggest or provide motivation for removing the biasing and driving the biasing to a ground supply voltage during times when the differential signal is absent. Present claim 18 makes clear that whenever a differential signal is absent, the input to the CMOS inverter is biased to a ground supply voltage. Specifically, Fig. 3 illustrates a CMOS inverter 36a/36e that is biased to a ground supply via transistor 40 (Specification -- Fig. 3). Nowhere is there any suggestion in Iida for biasing the input of inverter 20 to a ground supply during times

when a differential signal is absent (Iida – Fig. 3). Accordingly, Applicants assert that independent claim 18 and claims dependent therefrom are not obvious over Iida.

For at least the reasons stated above, Applicants believe independent claims 1, 11, and 18, as well as claims dependent therefrom, are patentably distinct over the cited art. Accordingly, removal of this rejection is respectfully requested.

CONCLUSION

The present amendment and response is believed to be a complete response to the issues raised in the Office Action mailed September 16, 2005. In view of the remarks herein traversing the rejections, Applicants assert that pending claims 1-4, 6, and 8-19 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned earnestly requests a telephone conference.

Applicant respectfully petitions the Commissioner for a one month extension of time under 37 C.F.R. § 1.136 for submitting a response to the Office Action mailed September 16, 2005, such extension allowing the undersigned until January 16, 2006 to respond.

The Commissioner is authorized to charge the required fees or credit any overpayment to Daffer McDaniel, LLP Deposit Account No. 50-3268/5298-13101.

Respectfully submitted,

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